CPU Supervisors: Frequently Asked Questions

Addresses the function of a CPU supervisor and how they can be applied to monitor a system. Discusses the function of a watchdog timer, chip enable gating pin, as well as a sense input for an early warning signal. The document also focuses on the difference between a reset circuit and a voltage detector and how to choose the proper voltage threshold.

What Is A Watchdog Used For?

The watchdog timer feature found on many CPU Supervisors allows the supervisor to monitor and restart a processor based on its operation. In simplest terms, all the watchdog timer does is restart a clock each time a transition on its input occurs. If the clock times out, then a reset or watchdog status output goes active. The input for the watchdog can be derived from many processor or system signals. Some of the most commonly used include data/address I/Os and Interrupt outputs. In many cases a processor stalls because of a power transient, data, or software error. Monitoring processor operation can allow the supervisor to restart a stalled processor when no actual system problem exists. This provides for cost savings in system service personnel and can reduce down time.

What Is The Difference Between A Reset And A Voltage Detector?

Voltage detectors simply indicate that a voltage is above or below a specific value. They do not provide any timing delays and generally have very limited noise immunity. Resets provide a digital signal to the processor that not only indicates the voltage level but also provides that the reset signal is delayed to allow the voltage to arrive at its nominal value. That delay also allows the power supply and board to fully stabilize prior to starting operation.

What CPU Supervisor Device Tolerance Should Be Used For Best Results?

This is a matter of personal preference as much as engineering necessity. Generally speaking, the reset tolerance should be set below the worst-case operation of the power supply. This means a 5-volt power supply rated at ±10% would typically be used with a 5-volt 10% tolerance supervisor. Although a 5%

supervisor could be used in this application, the possibility exists that spurious resets could be generated under normal conditions. Also, a 5-volt 15% supervisor might be used to provide for greater noise or actual power conditions at the supervisor location, which are generally going to be worse than the conditions at the power supply output. Consideration of operating voltages for system components is also important. However, because supervisors provide a delay on power-up, in many cases they are less critical in this selection process.

I need A Dual 5V Reset. What Do You Have?

The 1834 can have 5V applied to the 3.3V side in order to have two resets with different trip points. If a resistor divider is used, at least 10mA of current should be available to the input.

What Does Device Tolerance Refer To In CPU Supervisors?

Device tolerance can be used to refer to two different device values. One is the voltage value at which the device recognizes that power is good. This is the way Dallas Semiconductor uses the term. Generally, it would be indicated as simply a percentage (For example, 5%) and would indicate the device will trip just below the operating voltage minus 5%. The other value that is sometimes referred to as the tolerance is the variation or the accuracy of the trip value around its center point. In most cases this would be referred to as plus-or-minus some percentage (e.g., 2%). Generally, most products supplied by Dallas Semiconductor operate with a 2% around the trip level or 2.5 around the specified operating voltage.

What Is A Sense Input And NMI Output?

These refer to the (Sense) Input and Non-Maskable Interrupt (NMI) output of referenced comparators that are found on many of the CPU Supervisor products. They can be configured to monitor an upstream voltage in order to provide an early warning of an impending power failure, allowing time to save critical data. In this application, the NMI output would generally be connected to a NMI input of a processor. They are also used to monitor secondary system voltages and provide a "system not ready" indicator to provide more consistent system operation. In this application, the NMI output can be connected to a processor interrupt, pushbutton reset input, or other control inputs.

What Are CEI And CEO Pins On Many Of The CPU Supervisory Components?

Chip Enable Input (CEI) and Chip Enable Output (CEO) provide a method to

control RAM chip enable based on the value of V_{CC}. The CEI is typically connected to a processor address output, RAM decode output, or directly to ground if the RAM is always enabled. The CEO is typically connected to the CE input on the RAM. This allows the RAM to be automatically de-selected if the voltage on V_{CC} is below the rated value protecting data during power transients. If not used, CEI would typically be connected to ground and CEO would be left floating.

What Is The Largest Capacitor Allowed For The Programmable Delay On The DS1238?

The maximum capacitor size for the programmable delay is determined by the maximum leakage current. The larger the capacitor, the higher quality that the capacitor has to be to keep the leakage current below 1mA or the capacitor will never charge.

More Information

DS1238: QuickView -- Full (PDF) Data Sheet -- Free Samples

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